Abstracts

ESD protection of RF circuits in standard CMOS process (2002 [RFIC])

K. Higashi, A.O. Adan, M. Fukumi, N. Tanba, T. Yoshimasu and M. Hayashi. "ESD protection of RF circuits in standard CMOS process (2002 [RFIC])." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 285-288.

The tradeoffs in the ESD protection device for RFCMOS circuits are described, and the characteristics of an SCR-based ESD structure are presented. The parasitic capacitance of the ESD structure is reduced to /spl sim/150 fF. 3 kV HBM and 750 V CDM are achieved in a LNA working at 2.5 GHz with NF<4dB, applicable for Bluetooth wireless transceiver.

❑ Return to main document.